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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/624,421	07/22/2003	Van D. Nguyen	400.191US01	7247

27073 7590 05/13/2008
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EXAMINER	
YU, JAE UN	

ART UNIT	PAPER NUMBER
2185	

MAIL DATE	DELIVERY MODE
05/13/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/624,421	NGUYEN, VAN D.	
	Examiner	Art Unit	
	JAE U. YU	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14,16,17,19 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14, 16, 17 and 19-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The examiner acknowledges the applicant's submission of RCE dated 4/21/2008. At this point claims 1, 7, 11, 13, 17 and 20 have been amended. Claims 15 and 18 have been cancelled. Thus, claims 1-14, 16, 17 and 19-20 are pending in the instant application.

Response to Amendment

In view of the applicant's amendment, the double patenting rejection for claims 11-14, 16, 17, 19 and 20 are withdrawn. The examiner directs the applicant's attention the following new ground(s) of rejection.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 1, 7, 11, 13, 17 and 20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 1, 7, 11, 13, 17 and 20 recite, "replace a single designed (flash) memory device, over a contiguous range of logical memory addresses". Nowhere in the

specification discloses that the memory being replaced is a flash and such memory has the "contiguous range of logical memory address". Thus, the claim introduces a new matter. Further, the claims recite, "each non-contiguous physical memory address space corresponds to a different memory device of the multiple memory devices". However, nowhere in the specification discloses that each flash memory devices includes a non-contiguous address sub-range. Upon expecting the specification, especially paragraph 35, the examiner concludes that the sub-ranges are non-contiguous because they are materialized in a plurality of different memory devices, not because each of the plurality of memory devices contains a non-contiguous address range within itself.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-14, 16, 17 and 19-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Borkenhagen et al. (US 5,067,105) in view of Daberko (US 5,787,445).

2. As per **independent claims 1, 7, 11, 13, 17 and 20**, Borkenhagen et al. discloses, "receiving a command comprising a first logical memory address **[Receiving**

a logical card memory address, Column 3, Lines 60-64] from the range of logical memory addresses **[Logical Memory addresses, Column 3, Lines 60-64]**".

"accessing a look-up table having logical memory addresses with their corresponding physical memory addresses **[data structure comprising logical cards and physical cards, Figure 2, Borkenhagen et al.]** from one of the plurality of physical memory address to find a first physical memory address, from a range of physical memory addresses, that corresponds to the first logical memory address **[Determining a physical card memory address that corresponds to the logical card memory address, Figure 2, (Column 3, Line 65 – Column 4, Line 10)]**"

"Generating a chip select signal to one of the plurality of the multiple memory devices in response to the first physical memory address **[Selecting a physical card based on the physical card memory address, (Column 3, Line 65 – Column 4, Line 10), Figure 1)]** wherein the plurality of ranges of physical memory addresses include non-contiguous physical memory address space such that each non-contiguous physical memory address space corresponds to a different memory device of the multiple memory devices **[independent physical storage cards, Figure 2]**".

Borkenhagen et al. do not disclose expressly, "the single flash memory device having the contiguous range of logical memory addresses".

Daberko discloses, "flash RAM" in column 3, at lines 14-16.

Borkenhagen et al. and Daberko are analogous art because they are from the same filed of endeavor of increasing fault tolerance by memory access control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Borkenhagen et al. by including a "flash RAM" as taught by Daberko in column 3, at lines 14-16.

The motivation for doing so would have been increased fault tolerance to power interruption as expressly taught by Daberko in column 3, at lines 23-25.

Therefore, it would have been obvious to combine Daberko with Borkenhagen et al. for the benefit of increased fault tolerance to obtain the invention as specified in claims 1, 7, 11, 13, 17 and 20.

3. **Claim 2** discloses, "the range of physical memory addresses is contiguous **["physical memory addresses" sharing the same "physical card memory address", (Column 3, Line 65 – Column 4, Line 10), Figure 1)]**".

4. **Claim 3** discloses, "the range of physical memory addresses is substantially equivalent to the range of logical memory addresses **[The "logical memory address" and the corresponding "physical memory address" are identical except the first 3-bits (The identical memory addresses are materialized in a different physical memory card), (Column 3, Line 60 – Column 4, Line 10)]**".

5. **Claim 5** discloses, "the range of logical memory addresses are contiguous and the corresponding range of physical memory addresses is non-contiguous and comprised of a plurality of physical sub-ranges **["physical memory addresses materialized in a plurality of physical memory cards, Figure 2]**".

6. **Claim 6** discloses, "a chip select signal **[Selecting a physical card based on the physical card memory address, (Column 3, Line 65 – Column 4, Line 10), Figure 1)]** is generated for each physical memory address sub-range **["physical memory addresses materialized in a plurality of physical memory cards, Figure 2]**".

7. **Claim 7** discloses, "receiving a command comprising a first logical memory address **[Receiving a logical card memory address, Column 3, Lines 60-64]** from the range of logical memory addresses **[Logical Memory addresses, Column 3, Lines 60-64]**".

"accessing a look-up table having logical memory addresses with their corresponding physical memory addresses **[data structure comprising logical cards and physical cards, Figure 2, Borkenhagen et al.]** from one of ranges of physical memory addresses to find a first physical memory address, from a range of non-contiguous physical memory addresses **["physical memory addresses materialized in a**

plurality of physical memory cards, Figure 2], that corresponds to the first logical memory address **[Determining a physical card memory address that corresponds to the logical card memory address, Figure 2, (Column 3, Line 65 – Column 4, Line 10)]**"

"Generating a chip select signal in response to the first physical memory address **[Selecting a physical card based on the physical card memory address, (Column 3, Line 65 – Column 4, Line 10), Figure 1)]**"

8. **Claim 8** discloses, "a controller circuit executing an application in which the first logical memory address is read from memory **[CPU executing an application and generating a logical memory address, Figure 1, Column 3, Lines 60-68]** along with the command".

9. **Claim 9** discloses, "a device manager receiving the first logical memory address **[Physical card selector logic receiving the first logical memory address, Figure 1]** from a controller circuit".

10. **Claim 10** discloses, "the device manager generates the chip select signal **[Physical card selector logic selecting appropriate chip, Figure 1, (Column 3, Line 65 – Column 4, Line 10)]** in response to the first physical memory address".

11. As per **claim 4**, **Daberko discloses, "flash RAM" in column 3, at lines 14-16.**

12. **Claim 12** discloses, "the plurality of non-contiguous sub-ranges is substantially equal to a logical memory address range of a flash memory device **[The "logical memory address" and the corresponding "physical memory address" are identical except the first 3-bits (The identical memory addresses are materialized in a different physical memory card), (Column 3, Line 60 – Column 4, Line 10)]**".

13. **Claim 14** discloses, "the controller circuit is coupled to the plurality of flash memory through a plurality of memory address lines **[Figure 3C, Daberko]**".

14. **Claims 16 and 19** disclose, "the controller circuit generates the first physical memory address in response to adding a memory address offset to the first logical memory address **[the difference between the generated physical memory address and the logical memory address is the "offset", Figure 1]**".

Arguments Regarding Prior Art Rejections

1st Point of Argument

Regarding the independent claims, the applicant argues that the cited references fail to teach the new limitation of "replacing the single flash memory device having the contiguous range of logical memory addresses with the plurality of flash memory devices". However, Daberko discloses a "flash RAM" in column 3, lines 14-16, and

Borkenhagen discloses such "plurality of flash memory devices". Thus, the combination of Daberko and Borkenhagen expressly teaches every claimed element.

Further, the applicant argues that the cited references fails to teach the new limitation of each of the plurality of memory devices has a physical address sub-ranges. However, Borkenhagen clearly discloses such "sub-range" in each of the physical memory devices depicted in Figure 2.

Conclusion

A. Claims No Longer in the Application

Claims 15 and 18 are cancelled.

B. Claims Rejected in the Application

Claims 1-14, 16, 17 and 19-20 have received a first action on the merits and are subject of a first action non-final.

C. Direction of Future Remarks

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jae Un Yu who is normally available from 9:00 A.M. to 5:30 P.M. Monday thru Friday and can be reached at the following telephone number: (571) 272-1133.

If attempts to reach the above noted examiner by telephone are unsuccessful, the Examiner's supervisor, Sanjiv Shah, can be reached at the following telephone number: (571) 272-4098.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jae U Yu/

Examiner, Art Unit 2185

5/10/2008

/Sanjiv Shah/

Supervisory Patent Examiner, Art Unit 2185